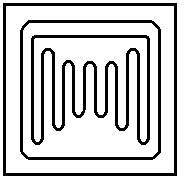
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.122”**



**E**

**B**

**.122”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .020” X .020”**

**Backside Potential: COLLECTOR**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .122” X .122” DATE: 4/20/18**

**MFG: MOTOROLA THICKNESS .015” P/N: 2N5153**

**DG 10.1.2**

#### Rev B, 7/1